What is claimed is:

1. An array printed circuit board, comprising:

at least one circuit board having a first surface, a first layout of first and second chip mounting regions formed on a first half of the first surface and a second layout of first and second chip mounting regions formed on a second half of the first surface, the first and second layouts having opposite first and second chip mounting region patterns.

2. The array printed circuit board of claim 1, wherein the first layout provides for alternating first and second chip mounting regions beginning with the first chip mounting region and the second layout provides for alternating first and second chip mounting regions beginning with the second chip mounting region.

3. The array printed circuit board of claim 2, wherein the first and second chip mounting regions have different layouts.

4. The array printed circuit board of claim 1, wherein the first and second chip mounting regions have different layouts.

5. The array printed circuit board of claim 1, further comprising:

a number of the circuit boards sequentially connected to one another in a direction perpendicular to a direction in which the first and second chip mounting regions arrayed on each circuit board.

6. The array printed circuit board of claim 1, wherein the circuit board has a second surface opposite the first surface, the second surface has a first half disposed under the first half of the first surface and a second half disposed under the second half of the first surface, the second layout formed on the first half of the second surface and the first layout formed on the second half of the second surface.

7. The array printed circuit board of claim 6, wherein the first layout provides for alternating first and second chip mounting regions beginning with the first

chip mounting region and the second layout provides for alternating first and second chip mounting regions beginning with the second chip mounting region.

8. The array printed circuit board of claim 7, wherein the first and second chip mounting regions have different layouts.

9. The array printed circuit board of claim 6, wherein the first and second chip mounting regions have different layouts.

10. The array printed circuit board of claim 6, further comprising:

a number of the circuit boards sequentially connected to one another in a direction perpendicular to a direction in which the first and second chip mounting regions arrayed on each circuit board.

11. The array printed circuit board of claim 1, further comprising:

a number of the circuit boards sequentially connected to one another in

a direction perpendicular to a direction in which the first and second chip mounting regions arrayed on each circuit board.

12. An array printed circuit board, comprising:

at least one circuit board having a front and rear surface, the front surface having a first pattern of first and second chip mounting regions and the rear surface having a second pattern of first and second chip mount regions, the second pattern being an opposite of the first pattern.

13. The array printed circuit board of claim 12, wherein the first pattern provides for alternating first and second chip mounting regions beginning with the first chip mounting region and the second pattern provides for alternating first and second chip mounting regions beginning with the second chip mounting region.

14. The array printed circuit board of claim 13, wherein the first and second chip mounting regions have different layouts.

15. The array printed circuit board of claim 13, further comprising:

a number of the circuit boards sequentially connected to one another in a direction perpendicular to a direction in which the first and second chip mounting regions arrayed on each circuit board.

16. The array printed circuit board of claim 12, wherein the first and second chip mounting regions have different layouts.

17. The array printed circuit board of claim 12, further comprising:

a number of the circuit boards sequentially connected to one another in a direction perpendicular to a direction in which the first and second chip mounting regions arrayed on each circuit board.